

EDA Linkage Software

Provide a front-to-Back software solution, which shortens the turn around time(TAT) of SoC tests.

ADVANTEST provides the software tools, which totally supports device tests for design, evaluation, analysis, failure diagnostics, and yield improvement on the Viewpoint software platform.

Good Performance

The tool transforms design data into the test resource at high speed and the automation is also possible. Seamless connecting of the gap of design and test reduces the customer's work greatly.

Good Operation

Provides an operational environment based on a GUI, where continuous operation is possible. Effective work is possible without any thought disturbance.

Good Investment

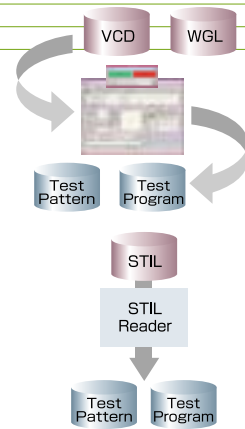
ADVANTEST's tool can be combined with the customer tools. It effects reasonable cost performance.

CATVert

This tool converts LSI design data(VCD) and DFT data(WGL) into ATE test pattern and test program with high speed and simple operation.

STIL Reader

This tool converts LSI design data(STIL:IEEE1450) into ATE test pattern and test program with high speed and simple operation.

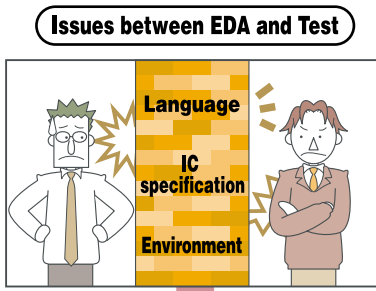
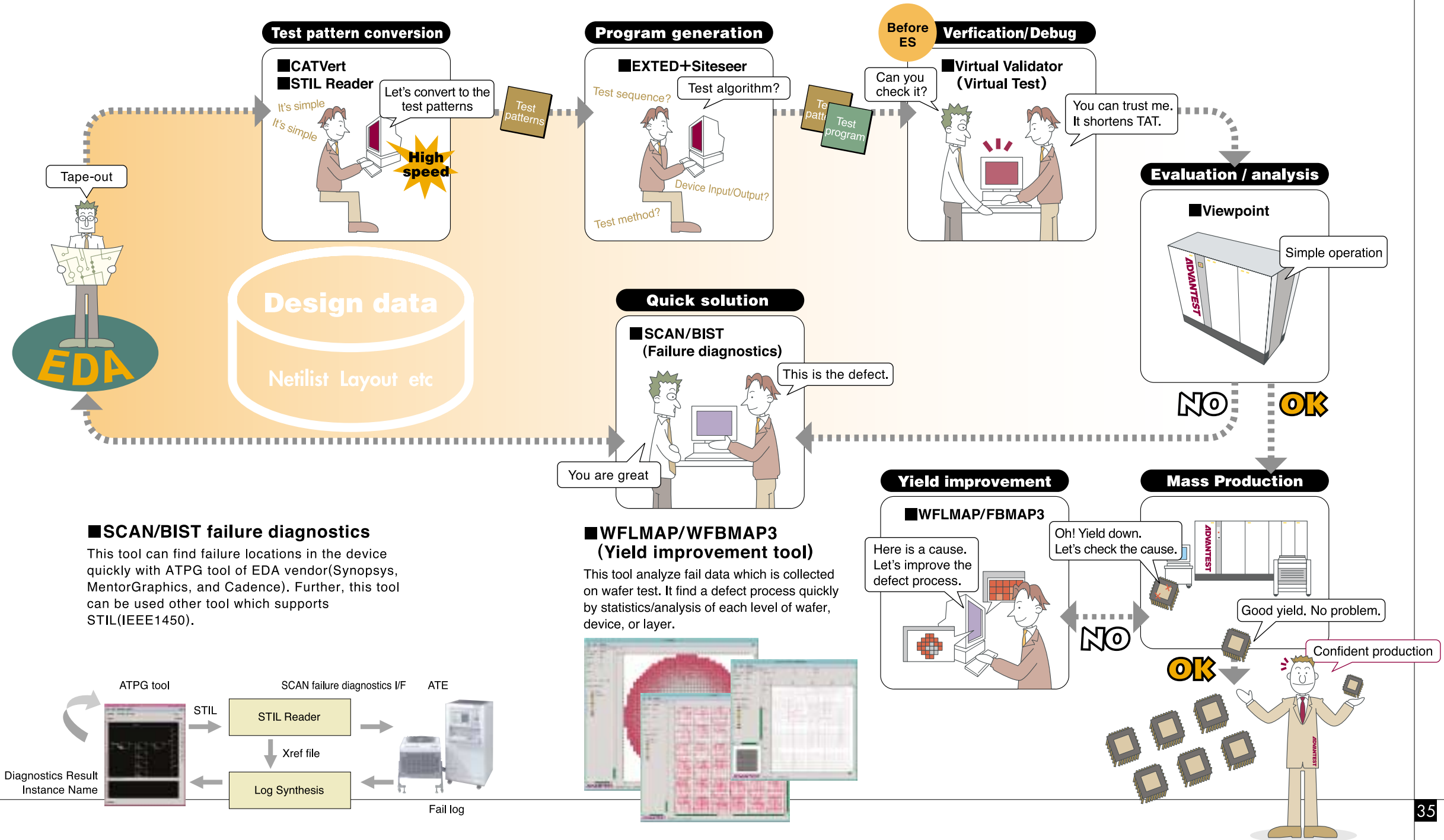
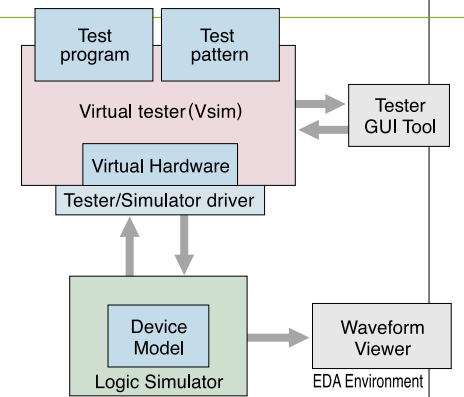


EXTED+Siteeer

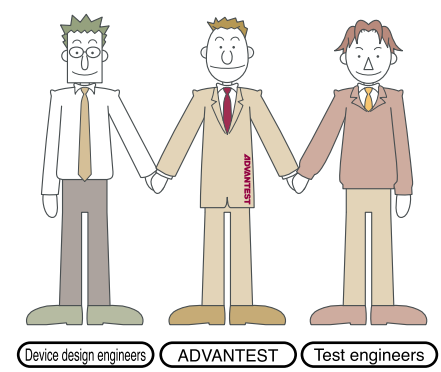
This tools generate test program by using Excel with simple operation.

Virtual Validator (Virtual test)

The test programs and test patterns can be validated before engineering sample(ES) are made. It shortens the turn around time(TAT) greatly.

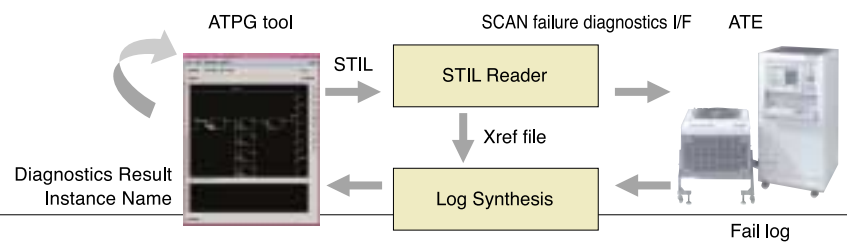


From now on



SCAN/BIST failure diagnostics

This tool can find failure locations in the device quickly with ATPG tool of EDA vendor(Synopsys, MentorGraphics, and Cadence). Further, this tool can be used other tool which supports STIL(IEEE1450).



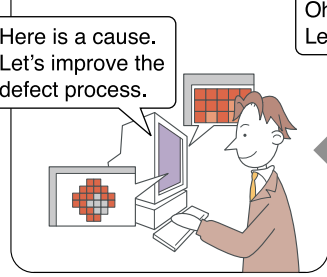
WFLMAP/WFBMAP3 (Yield improvement tool)

This tool analyze fail data which is collected on wafer test. It find a defect process quickly by statistics/analysis of each level of wafer, device, or layer.



Yield improvement

WFLMAP/WFBMAP3



Mass Production

WFLMAP/WFBMAP3

